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FROM: Peter Yim
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DATE: February 28, 2006

Number of pages with cover page:	21	

Preparer of this slip has confirmed that facsimile number given is correct: **PJY1/8566**

CAUTION - CONFIDENTIAL

Comments:

PLEASE PROCESS THE ATTACHED.

Re: U.S. Patent Application Serial No. 10/664,783
For: ELECTROPOLISHING METAL LAYERS ON WAFERS HAVING TRENCHES OR VIAS WITH DUMMY STRUCTURES
By: Hui WANG et al.
Our Reference: 49515-20006.10

Attached is the following:

1. Transmittal (1 Page)
2. Fee Transmittal (in duplicate, 2 pages)
3. Petition for Extension of Time (1 page)
4. Appeal Brief (16 pages)

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PTO/SB/21 (08-00)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

		Application Number	10/664,783
		Filing Date	September 16, 2003
		First Named Inventor	Hui WANG
		Group Art Unit	2623
		Examiner Name	M. Estrada
Total Number of Pages in This Submission	20	Attorney Docket Number	495152000610

ENCLOSURES (*check all that apply*)

[x] Fee Transmittal Form (in duplicate, 2 pages)	[ ] Assignment Papers *(for an Application)*	[ ] After Allowance Communication to Group
[ ] Fee Attached	[ ] Drawing(s)	[ ] Appeal Communication to Board of Appeals and Interferences
[ ] Amendment/Reply	[ ] Licensing-related Papers	[x] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief) (16 pages)*
[ ] After Final	[ ] Petition	[ ] Proprietary Information
[ ] Affidavits/declaration(s)	[ ] Petition to Convert to a Provisional Application	[ ] Status Letter
[x] Extension of Time Request (1 page)	[ ] Power of Attorney, Revocation Change of Correspondence Address	[x] Other Enclosure(s) *(please identify below)*
[ ] Express Abandonment Request	[ ] Terminal Disclaimer	Facsimile Cover Sheet (not counted as part of this submission)
[ ] Information Disclosure Statement	[ ] Request for Refund	
[ ] Certified Copy of Priority Document(s)	[ ] CD, Number of CD(s) _____	
[ ] Response to Missing Parts/ Incomplete Application	Remarks	
[ ] Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual Name	MORRISON & FOERSTER LLP (Customer No. 20872) Peter J. Yim – 44,417
Signature	Peter J. Yim
Date	February 28, 2006

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Dated: February 28, 2006 Signature: Peter J. Yim (Peter Yim)

sf-2088105

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

[X] Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,045

Complete if Known	
Application Number	10/664,783
Filing Date	September 16, 2003
First Named Inventor	Hui WANG
Examiner Name	M. Estrada
Art Unit	2823
Attorney Docket No.	495152000610

METHOD OF PAYMENT (check all that apply)

[ ] Check [ ] Credit Card [ ] Money Order [ ] None [ ] Other (please identify): _____

[X] Deposit Account Deposit Account Number: 03-1952 Deposit Account Name: Morrison & Foerster LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

[X] Charge fee(s) indicated below [ ] Charge fee(s) indicated below, except for the filing fee

[X] Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 [X] Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
50	-50 = 0	x 25	= 0.00

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
180	0.00

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
3	-3 = 0	x 100	= 0.00

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(c)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
- 100 =	/50	(round up to a whole number) x	=	0.00

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 2402 Filing a brief in support of an appeal	250.00
2254 Extension for Response Within Fourth Month	795.00

SUBMITTED BY

Signature	Pet J. Yim	Registration No. (Attorney/Agent) 44,417	Telephone (415) 268-6373
Name (Print/Type)	Peter J. Yim		Date September 15, 2005

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Dated: February 28, 2006 Signature: (Peter Yim)

Docket No.: 495152000610
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hui WANG et al.

Application No.: 10/664,783

Filed: September 16, 2003

Art Unit: 2823

For: ELECTROPOLISHING METAL LAYERS ON WAFERS HAVING TRENCHES OR VIAS WITH DUMMY STRUCTURES

Examiner: M. Estrada

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This brief is accompanied by a 1.136(a) petition for a four-month extension of time and appropriate 1.17(a) fee. Thus this brief is timely filed, as required under § 41.37(a), and is in furtherance of the Notice of Appeal filed on September 15, 2005.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party in Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal

PAGE 6/21 * RCVD AT 2/28/2006 8:21:13 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:2738300 * CSID:415 2687522 * DURATION (mm-ss):06-10

03/02/2006 EFLORES 00000056 031952 10664783
01 FC:2402 250.00 DA

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

ACM Research, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 50 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-10.
2. Claims withdrawn from consideration but not canceled: 0.
3. Claims pending: 11-60.
4. Claims allowed: 31-43.
5. Claims rejected: 11, 15, 16, 21-24, 28-30, 44, 47, 48, 52-55, and 58-60.
6. Claims objected to: 12-14, 17-20, 25-27, 45, 46, 49-51, 56, and 57.

C. Claims on Appeal

The claims on appeal are claims 11-30 and 44-60.

IV. STATUS OF AMENDMENTS

No Amendments have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 11 recites a structure formed on a semiconductor wafer. (Page 5, paragraph [0035], lines 1-3; Figs. 1A, 2A.) A dielectric layer is formed with a recessed area and a non-recessed area. (Page 5, paragraph [0036], lines 3-5, Figs. 1A, 2A.) A plurality of dummy structures are formed within the recessed area. (Page 7, paragraph [0043]; Fig. 2A.) The dummy structures are inactive areas configured to increase the planarity of a metal layer that is subsequently formed on the dielectric layer. (Page 2, paragraph [0006], lines 4-6.) A metal layer is formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures. (Page 8, paragraph [0048]; Fig. 2C.) The metal layer is electropolished to expose the non-recessed area. (Page 9, paragraph [0049]; Fig. 2D.)

Independent claim 44 recites a structure formed on a semiconductor wafer. (Page 5, paragraph [0035], lines 1-3; Figs. 1A, 2A, 3A.) A dielectric layer is formed with a recessed area and a non-recessed area. (Page 5, paragraph [0035], lines 3-5, Figs. 1A, 2A, 3A.) A plurality of dummy structures are formed within the recessed area. (Page 7, paragraph [0043]; Figs. 2A, 3A.) The dummy structures are inactive areas configured to increase the planarity of a metal layer that is subsequently formed on the dielectric layer. (Page 2, paragraph [0006], lines 4-6.) A metal layer is formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures. (Page 8, paragraph [0048]; Figs. 2C, 3C.) The metal layer is electropolished to expose the non-recessed area. (Page 9, paragraph [0049]; Figs. 2D, 3D.) The metal layer is overpolished to allow the non-recessed area to protrude past a surface of the metal layer in the recessed area. (Page 10, paragraph [0052], lines 6-9; Fig. 3D.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 11, 15, 24, and 29 are anticipated under 35 U.S.C. 102(e) as by U.S. Patent No. 6,653,226 (the Reid reference).

B. Whether claims 16, 21-23, 28, 30, 44, 47, 48, 52-55, 58, 59, and 60 are unpatentable under 35 USC 103(a) over the Reid reference in further view of U.S. Patent No. 6,383,917 (the Cox reference).

VII. ARGUMENT

Claims 11, 15, 16, 21-24, 28-30, 44, 47, 48, 52-55, and 58-60 were finally rejected by the Examiner in a Final Office Action mailed on May 26, 2005. Applicants respectfully request reversal of the rejection of these claims in view of the following remarks.

A. <u>Claims 11, 15, 24, and 29.</u>

Claims 11, 15, 24, and 29 stand rejected under 35 U.S.C. 102(e) as being anticipated by the Reid reference. Applicants assert that the Examiner's 102(e) argument, based on Figure 1A of the Reid reference, is inconsistent with the teachings of the Reid reference and contrary to principles set forth in the MPEP.

The Examiner concluded in the Advisory Action mailed on August 4, 2005, stating that "features 107 and 109 [of Figure 1A] do the same function as the dummy structure of the instant application." This conclusion is inconsistent with the teachings of the Reid reference.

In particular, the Reid reference states that 107 features "are typically used for conductive lines and vias," and 109 features "are typically used for contact pads." (Column 1, lines 59-60, 62.) In contrast, the dummy structures of the instant application are explicitly recited in claim 11 as being "inactive areas." One skilled in the art would readily conclude that conductive lines and contact pads are "active areas" and could in no way be considered "inactive areas."

Note, in the Advisory Action, the Examiner has misinterpreted the Applicants' position in stating that "applicant argues that features 107 are *low* aspect ratio features and feature 109 is a low aspect ratio feature." The Applicants have consistently asserted in responses to both the first and final office actions that "107 features are *high* aspect ratio features."

Applicants also assert that the Examiner's arguments contradict important principles laid out in the MPEP. 37 CFR 1.84(p)(1) and MPEP 608.02(e) respectively state that: "the *same reference character must never be used to designate different parts*," and "the examiner should see to it . . . that *no single reference character is used for two different parts* or for a given part and a modification of such part." (Emphasis added.) The Examiner stated in the Advisory Action that "recesses in the area of 107 and 109 are as a whole the recessed are [sic] with dummy structures formed by dielectric 103. The farthest portion of dielectric 103 at the right after the area 109, is the non-recessed area." This argument differentiates some 103 structures from others in name and function by labeling several 103 features as "dummy structures" and others as non-recessed areas. This argument conflicts with 37 CFR 1.84(p)(1) and MPEP 608.02(e).

The Applicants further assert that the Examiner's arguments are contrary to the teachings and labeling system of the Reid reference. In FIG. 1A of the Reid reference, which is reproduced below, reference number 103 is used to reference dielectric layer 103, reference number 107 is used to reference high aspect ratio features, typically conductive lines, and reference number 109 is used to reference low aspect ratio features, typically used for contact pads. While the Applicants adopted Reid's Figure 1A and its terminology without alteration, the Examiner's departure contradicts Reid's figure and descriptions by merging four distinct 107 recessed areas with the 109 recessed area to form one large recessed area. Firstly, the Reid reference defines high aspect ratio features 107 as having "larger depth than width." If the four high aspect ratio features 107 in FIG. 1A were a single recessed area, the single large recessed area would cease to be a high aspect feature, as defined in Reid, because in having a larger width than depth it would be a low aspect ratio feature. Secondly, the Reid reference discloses that the high aspect ratio features 107 are typically used for conductive lines and vias. Therefore, in accordance with the teachings of the Reid reference, when

viewed from above the high aspect ratio features 107 would appear as distinct recessed areas rather than parts of a single large recessed area envisioned by the Examiner.

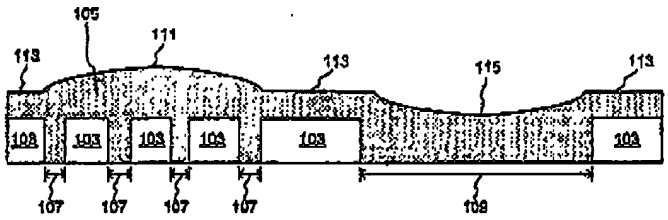

Figure 1A of the Reid reference

Independent claim 11 recites that the dielectric layer is formed having a recessed area and a non-recessed area, and that dummy structures are formed within the recessed area. In contrast, as can be seen from above, FIG. 1A of the Reid reference depicts four high aspect ratio features 107 and one low aspect ratio feature 109 formed as recessed areas in dielectric layer 103. The remnant portions of dielectric layer 103 in FIG. 1A correspond to the non-recessed area and not the dummy structures recited in claim 11. Because claim 11 recites that a dummy structure is formed within a recessed area, a dummy structure should appear in FIG. 1A as being formed within the low aspect ratio feature 109 or one of the four high aspect ratio features 107.

Furthermore, while FIG. 2A of the present application may appear to be similar to the portion of FIG. 1A of the Reid reference depicting high aspect ratio features 107, Applicants note that the similarity results from the fact that both are cross sectional views. As set forth in paragraph [0054] of the present application, FIG. 4 depicts an exemplary recessed area 100 that is a wide trench structure from a top view. As can be seen from FIG. 4, recessed area 100 is a single feature with dummy structures 200 disposed within it. In contrast, for the reasons set forth above, a corresponding top view of FIG. 1A from the Reid reference would show high aspect ratio features 107 as being distinct recessed areas.

For all of the reasons above, Applicants assert that claim 11 is allowable over the Reid reference. Applicants also assert that claims 15, 24 and 29 are allowable for at least the reason that they depend from an allowable independent claim.

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B. Claims 16, 21-23, 28, 30, 44, 47, 48, 52-55, 58, 59, and 60

Claims 16, 21-23, 28, 30, 44, 47, 48, 52-55, 58, 59, and 60 were rejected under 35 USC 103(a) as being unpatentable over the Reid reference in further view of U.S. Patent No. 6,383,917 (the Cox reference).

Independent claim 44 recites that a dielectric layer is formed having a recessed area and a non-recessed area, and that dummy structures are formed within the recessed area. For the reasons set forth above, Applicants assert that the Reid reference does not disclose or suggest dummy structures formed within recessed areas formed in a dielectric layer. The Examiner has not asserted that the Cox reference discloses the dummy structures recited in claim 44.

Thus, Applicants assert that claim 44 is allowable over the combination of the Reid reference and the Cox reference. Additionally, Applicants assert that claims 47, 48, 52-55, 58, 59, and 60 are allowable for at least the reason that they depend from an allowable independent claim, claim 44. Similarly, Applicants assert that claims 16, 21-23, 28, and 30 are allowable for at least the reason that they depend from an allowable independent claims, claim 11.

C. Claims 12-14, 17-20, 25-27, 45, 46, 49-51, 56, and 57

Claims 12-14, 17-20, 25-27, 45, 46, 49-51, 56, and 57 were objected to as being dependent upon a rejected base claim. For the reasons set forth above, Applicants assert that these claims depend from allowable independent claims, claims 11 and 44.

VIII. CLAIMS APPENDIX

A list of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: February 28, 2006

Respectfully submitted,

By _____

Peter J. Yim
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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/664,783

Claims 1-10 (Canceled)

Claim 11 (Original): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer having a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area,

wherein the dummy structures are inactive areas configured to increase the planarity of a metal layer subsequently formed on the dielectric layer;

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the non-recessed area.

Claim 12 (Original): The structure of claim 11, wherein the recessed area has a depth corresponding to a thickness of the metal layer to remain within the recessed area after electropolishing and an offset height corresponding to a distance between a surface of the non-recessed area to be exposed after electropolishing and a surface of the metal layer to remain within the recessed area after electropolishing.

Claim 13 (Original): The structure of claim 12, further comprising removing the exposed non-recessed area to a depth equal to the offset height.

Claim 14 (Original): The structure of claim 13, wherein the offset height is between about 5 nanometers to about 100 nanometers.

Claim 15 (Original): The structure of claim 11, wherein the metal layer is formed by depositing the metal layer.

Claim 16 (Original): The structure of claim 11, wherein the metal layer is formed by electroplating the metal layer.

Claim 17 (Original): The structure of claim 11,
wherein each dummy structure in the plurality has a width,
wherein the metal layer has a thickness,
wherein the thickness is based on the metal layer formed on the non-recessed area, and
wherein a ratio of the width to the thickness is between about 0.1 to about 1.

Claim 18 (Original): The structure of claim 17, wherein the ratio is 0.3.

Claim 19 (Original): The structure of claim 11,
wherein dummy structures in the plurality are spaced apart from each other by a distance,
wherein the metal layer has a thickness,
wherein the thickness is based on the metal layer formed on the non-recessed area, and
wherein a ratio of the distance to the thickness is between about 1 to about 5.

Claim 20 (Original): The stucture of claim 19, wherein the ratio is less than 2.

Claim 21 (Original): The structure of claim 11, further comprising:

a barrier layer formed on the dielectric layer before forming the metal layer.

Claim 22 (Original): The structure of claim 11, further comprising:

a seed layer formed on the dielectric layer before forming the metal layer.

Claim 23 (Original): The structure of claim 11, further comprising:

a cover layer formed on the semiconductor wafer after electropolishing the metal layer.

Claim 24 (Original): The structure of claim 11, wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer.

Claim 25 (Original): The structure of claim 11, wherein the recessed area is a large rectangular structure configured to form a pad when filled with the metal layer.

Claim 26 (Original): The structure of claim 25, wherein the exposed non-recessed area is removed beyond a surface of the electropolished metal layer to form a pad that protrudes beyond the dielectric layer to facilitate contact between the pad and a probe used for electrical testing.

Claim 27 (Original): The structure of claim 25, wherein the large rectangular structure has rounded corners.

Claim 28 (Original): The structure of claim 11, wherein the metal layer is copper.

Claim 29 (Original): The structure of claim 11, wherein the plurality of dummy structures includes the same material as the dielectric layer.

Claim 30 (Original): The structure of claim 11, wherein the plurality of dummy structures includes a metal.

Claim 31 (Original): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer,

wherein the dielectric layer is formed with a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area;

a barrier layer formed to cover the recessed area, the non-recessed area, and the plurality of dummy structures; and

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the barrier layer deposited on the non-recessed area, and wherein the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

Claim 32 (Original): The structure of claim 31, wherein the exposed barrier layer and the non-recessed area of the dielectric layer have even surfaces after the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

Claim 33 (Original): The structure of claim 31, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a first rate and the non-recessed area is removed at a second rate.

Claim 34 (Original): The structure of claim 31, wherein the first rate is equal to the second rate.

Claim 35 (Original): The structure of claim 31, wherein the first rate is lower than the second rate.

Claim 36 (Original): The structure of claim 31, wherein the exposed barrier layer is removed at a third rate and wherein the non-recessed area of the dielectric is removed at a fourth rate.

Claim 37 (Original): The structure of claim 36, wherein the third rate is higher than the fourth rate.

Claim 38 (Original): The structure of claim 37, wherein the fourth rate is zero.

Claim 39 (Original): The structure of claim 36, wherein the fourth rate is higher than the third rate.

Claim 40 (Original): The structure of claim 39, wherein the third rate is zero.

Claim 41 (Original): The structure of claim 36, wherein the first rate is higher than the second rate.

Claim 42 (Original): The structure of claim 36, wherein the exposed barrier layer and the non-recessed area have even surfaces after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.

Claim 43 (Original): The structure of claim 36, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.

Claim 44 (Previously Presented): A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer having a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area,

wherein the dummy structures are inactive areas configured to increase the planarity of a metal layer subsequently formed on the dielectric layer; and

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the non-recessed area, and wherein the metal layer is overpolished to allow the non-recessed area to protrude past a surface of the metal layer in the recessed area.

Claim 45 (Previously Presented): The structure of claim 44, wherein a portion of the non-recessed area that protrudes past the surface is removed.

Claim 46 (Previously Presented): The structure of claim 45, wherein the portion of the non-recessed area removed has a thickness of between about 5 to about 100 nanometers.

Claim 47 (Previously Presented): The structure of claim 44, wherein the metal layer is formed by depositing the metal layer.

Claim 48 (Previously Presented): The structure of claim 44, wherein the metal layer is formed by electroplating the metal layer.

Claim 49 (Previously Presented): The structure of claim 44,
wherein the dummy structure has a width,
wherein the metal layer has a thickness,
wherein the thickness is based on the metal layer deposited on the non-recessed area, and
wherein a ratio of the width to the thickness is between about 0.1 to about 1.

Claim 50 (Original): The structure of claim 49, wherein the ratio is 0.3.

Claim 51 (Previously Presented): The structure of claim 44,
wherein the dummy structure is spaced apart from the non-recessed area by a distance,
wherein the metal layer has a thickness,
wherein the thickness is based on the metal layer deposited on the non-recessed area, and
wherein a ratio of the distance to the thickness is between about 1 to about 5.

Claim 52 (Previously Presented): The structure of claim 44, further comprising a barrier layer formed on the dielectric layer before the metal layer is formed.

Claim 53 (Previously Presented): The structure of claim 44, further comprising a seed layer formed on the dielectric layer before the metal layer is formed.

Claim 54 (Previously Presented): The structure of claim 44, further comprising a cover layer formed on the semiconductor wafer after the metal layer is electropolished.

Claim 55 (Previously Presented): The structure of claim 44, wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer.

Claim 56 (Previously Presented): The structure of claim 44, wherein the recessed area is a large rectangular structure configured to form a pad when filled with the metal layer.

Claim 57 (Previously Presented): The structure of claim 56, wherein the exposed non-recessed area beyond the surface of the metal layer is removed to form a pad that protrudes beyond the dielectric layer to facilitate contact between the pad and a probe used for electrical testing.

Claim 58 (Previously Presented): The structure of claim 44, wherein the metal layer is copper.

Claim 59 (Previously Presented): The structure of claim 45, wherein the dummy structure includes the same material as the dielectric layer.

Claim 60 (Previously Presented): The structure of claim 44, wherein the dummy structure includes a metal.